REMARKS

Applicants appreciate the detailed examination evidenced by the final Office Action mailed August 25, 2005 (hereinafter "final Office Action"), including the withdrawal of the rejections in the Office Action mailed April 4, 2005 and the indication that Claims 11-13 and 24-26 recite patentable subject matter. Applicants respectfully traverse the new rejections based on U.S. Patent Application Publication No. 2003/0085747 to Hein et al. (hereinafter "Hein") and U.S. Patent Application Publication No. 2003/018235 to Conway et al. (hereinafter "Conway") for at least the reason that Conway does not provide the teachings alleged in the Office Action.

The Office Action asserts that Hein teaches all of the recitations of Claims 1 and 14 except "the detailed structure of the fine delay unit (2) using interpolation technique having first and second circuits and a phase interpolator," but asserts that Fig. 2 of Conway shows "a fine delay unit using interpolation technique." Final Office Action, p. 3. The Office Action further asserts that "it would have been obvious . . . to implement Hein et al.'s delay unit (2) with the circuit arrangement of Conway et al." Applicants respectfully disagree, as the interpolator shown in Fig. 2 of Conway is a digital signal processing device that is not compatible with the delay control loop shown in Fig. 3 of Hein.

In particular, the interpolator 10 shown in Fig. 2 of Conway is a ***signal sample*** interpolator, not a ***phase*** interpolator. In particular, the interpolator 10 receives signal samples x_{ic}. The signal samples are passed through a finite impulse response (FIR) filter 12 that includes a series of delay elements 16 that provide a delay of one clock cycle each, such that the delay elements provide a means of storing a series of signal samples. See Conway, paragraph [0011]. The ***signal samples*** held by the respective delay elements 16 are multiplied by respective coefficients stored in a read-only-memory (ROM) 14. The coefficients stored in the ROM 14 provide a ***sinc*** function. See Conway, paragraph [0012]. The interpolator 10 is clearly a signal sample processing device, not a device for interpolating a ***clock signal***. Therefore, the interpolator 10 is not suitable for use as a variable clock delay circuit such at the delay unit 2 shown in Fig. 3 of Hein and, for at least these reasons, Hein and Conway cannot be combined in the manner proposed in the final Office Action. Therefore, the cited combination of Hein and Conway does not disclose or suggest the

recitations of independent Claims 1 and 14 and, for at least these reasons, Applicants submit that independent Claims 1 and 14 are patentable.

Applicants submit that dependent Claims 3-7, 10-13, 15-20, 23-26 and 29 are patentable at least by virtue of the patentability of the various ones of independent Claims 1 and 14 from which they depend. Applicants further submit that several other of the dependent claims are separately patentable, including Claims 11-13 and 24-26 identified in the Office Action as reciting patentable subject matter.

In rejecting Claim 5, which recites "wherein the phase control circuit is operative to cause the phase interpolator circuit to shift from one extreme of a delay range thereof towards another extreme of the delay range concurrent with a step change in delay through the variable delay circuit," the final Office Action asserts that such recitations are "inherently present in figure 3 of Hein et al." Final Office Action, p. 3. This contradicts the final Office Action's own admission that Hein does not shown a fine delay with interpolation. Moreover, there is no evidentiary basis for this assertion of inherency. Accordingly, the rejection of Claim 5 should be withdrawn for at least these additional reasons.

In rejecting Claims 7 and 20, the Office Action asserts that "the combination of Hein et al and Conway reference shows the phase interpolator as an analog interpolator (Saitoh's figure 6)." Final Office Action, p. 3. As noted above, Conway does not show a ***phase*** interpolator. Moreover, the interpolator 10 shown in Fig. 2 of Conway is a ***digital*** circuit, not an analog circuit; the ***digital*** values stored in the delay elements 16 are multiplied by ***digital*** values stored in the ROM 14 to produce ***digital*** values that are summed by the adder 20 to produce a sequence of ***digital*** values Y_k. Finally, the reference to Saitoh clearly is an error. For at least these additional reasons, the rejections of Claims 7 and 20 should be withdrawn.

Conclusion

Applicants submit that the rejections of the claims should be withdrawn for at least the reasons discussed above. Applicants submit that the claims are in condition for allowance, which is respectfully requested. Applicants encourage the Examiner to contact the undersigned by telephone to resolve any outstanding issues.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 25, 2005.

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